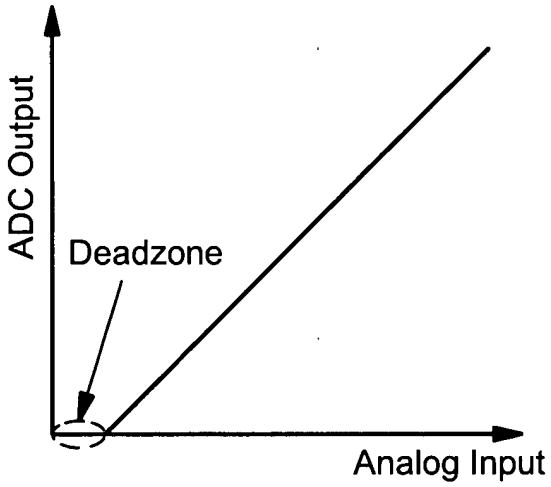
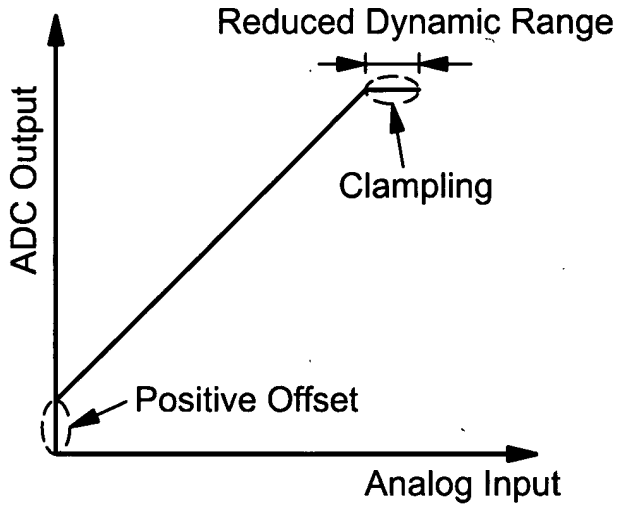
OIPE JC33
AUG 06 2004
PATENT & TRADEMARK OFFICE



Transfer Curve with Negative Offset

Figure 1



Transfer Curve with Positive Offset

Figure 2

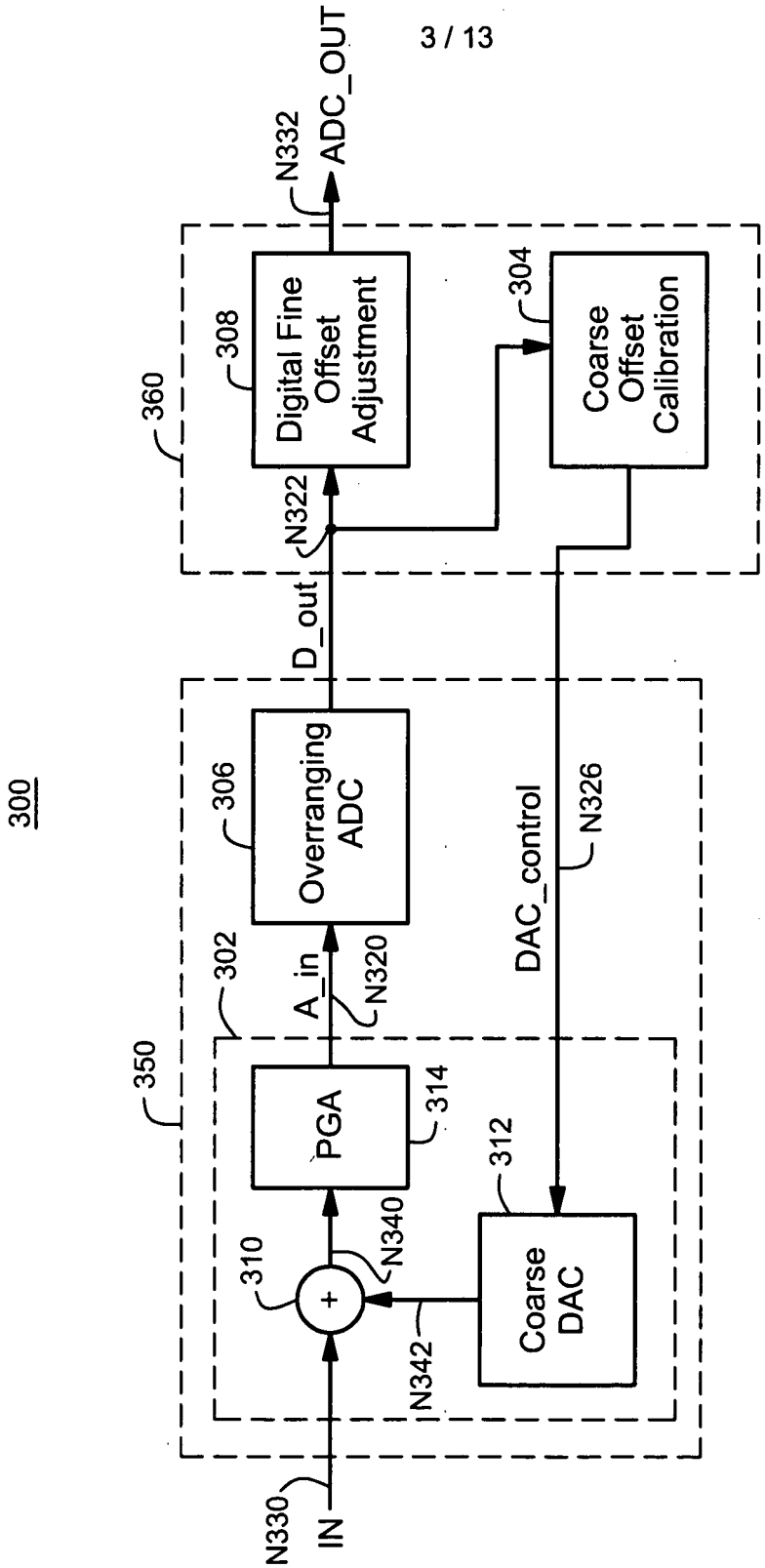

300
360
350
302
308
Digital Fine Offset Adjustment
304
Coarse Offset Calibration
306
Overranging ADC
310
PGA
314
312
Coarse DAC
N330
IN
N332
ADC_OUT
N322
D_out
N320
A_in
N326
DAC_control
N340
N342
+

Figure 3

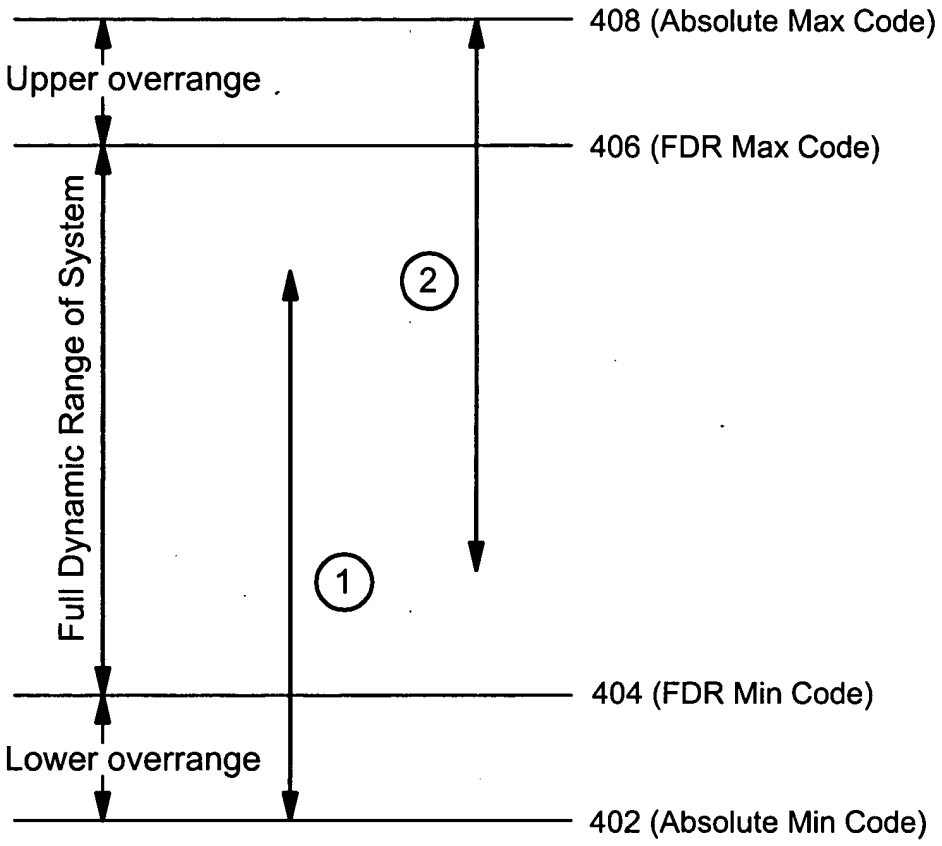

408 (Absolute Max Code)
Upper overrange
406 (FDR Max Code)
Full Dynamic Range of System
2
1
404 (FDR Min Code)
Lower overrange
402 (Absolute Min Code)

Figure 4

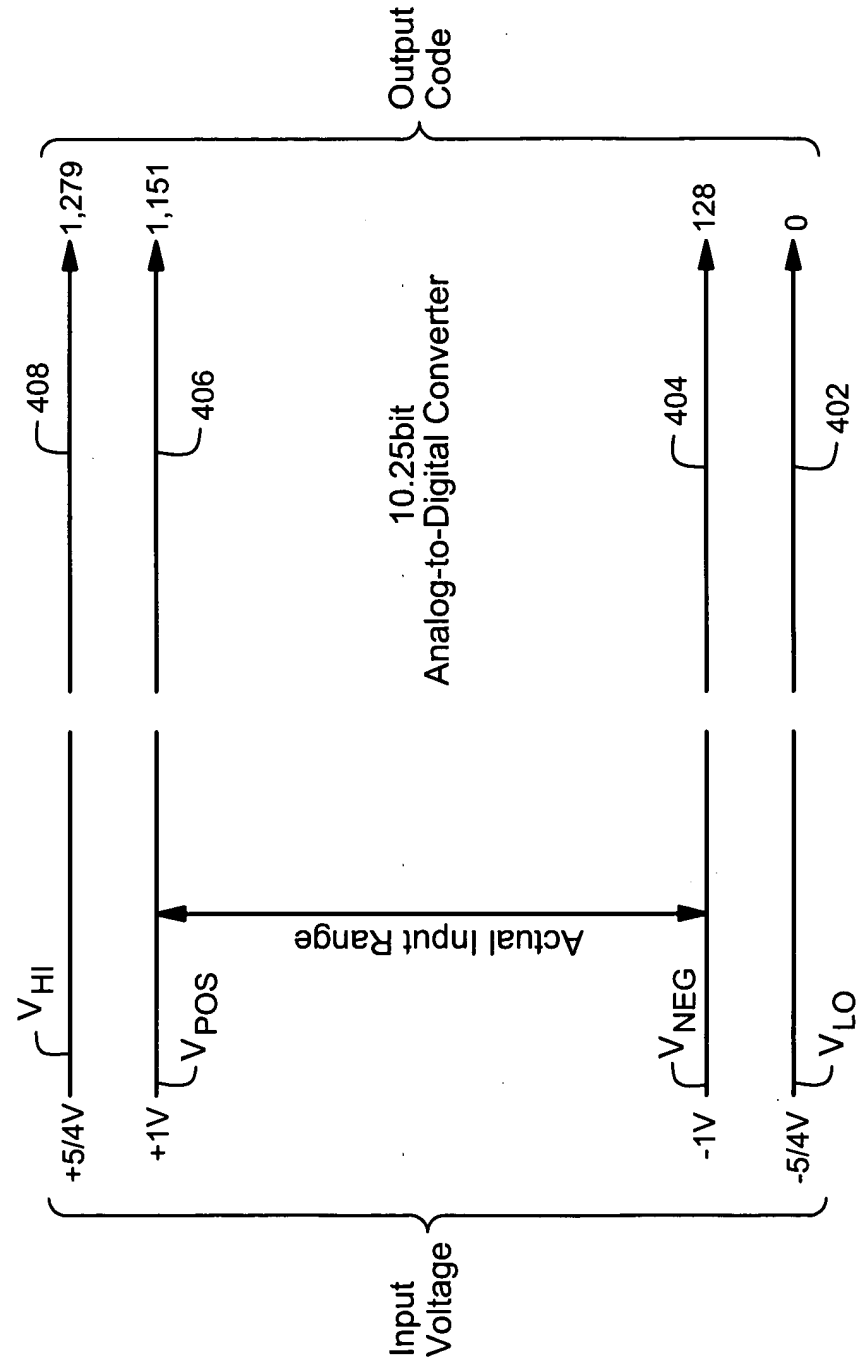

Output Code
1,279
1,151
128
0
408
406
404
402
10.25bit Analog-to-Digital Converter
Actual Input Range
V_{HI}
V_{POS}
V_{NEG}
V_{LO}
+5/4V
+1V
-1V
-5/4V
Input Voltage

Figure 5

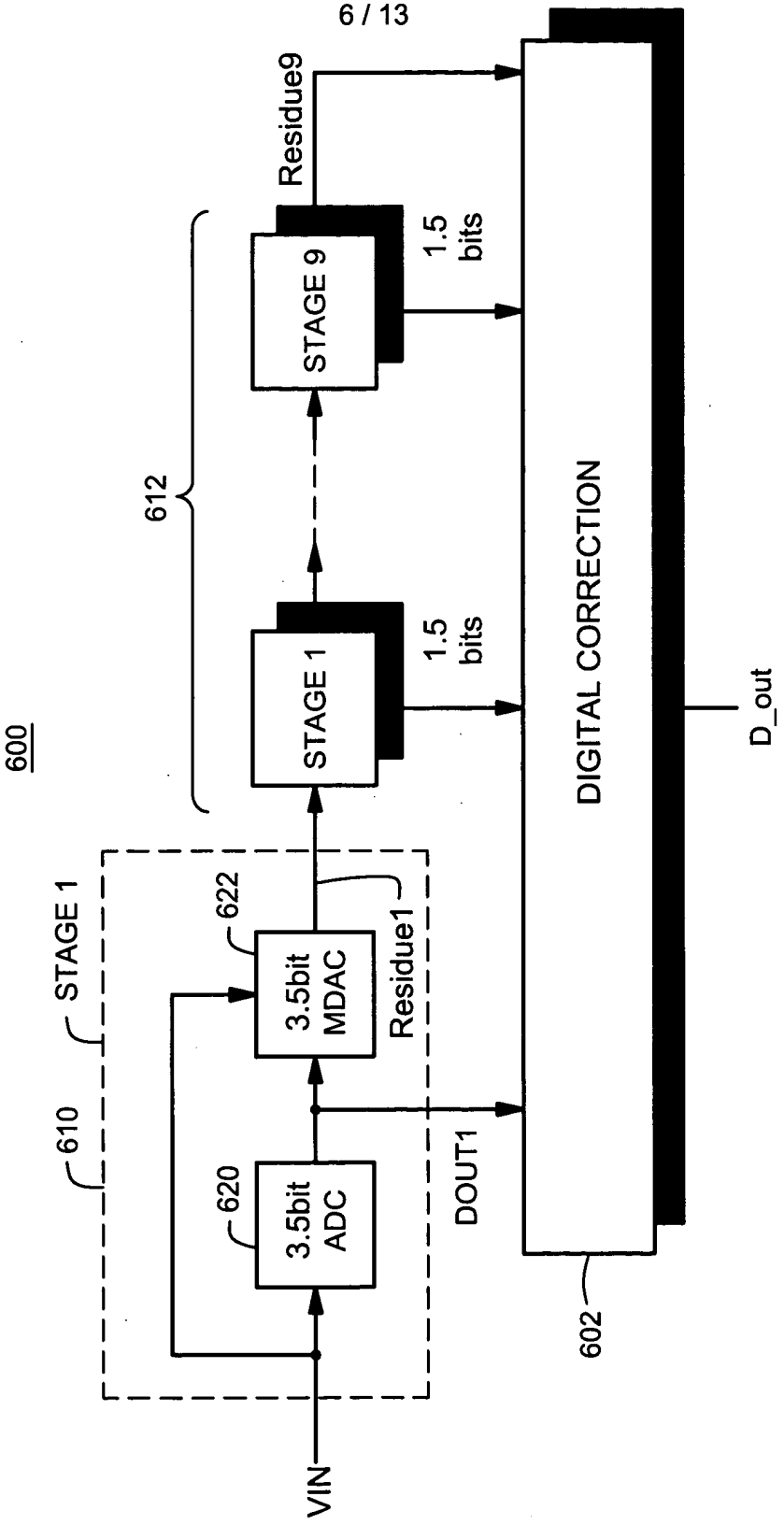

600
612
Residue9
STAGE 9
1.5 bits
STAGE 1
1.5 bits
DIGITAL CORRECTION
D_out
STAGE 1
622
3.5bit MDAC
Residue1
610
620
3.5bit ADC
DOUT1
602
VIN

Figure 6

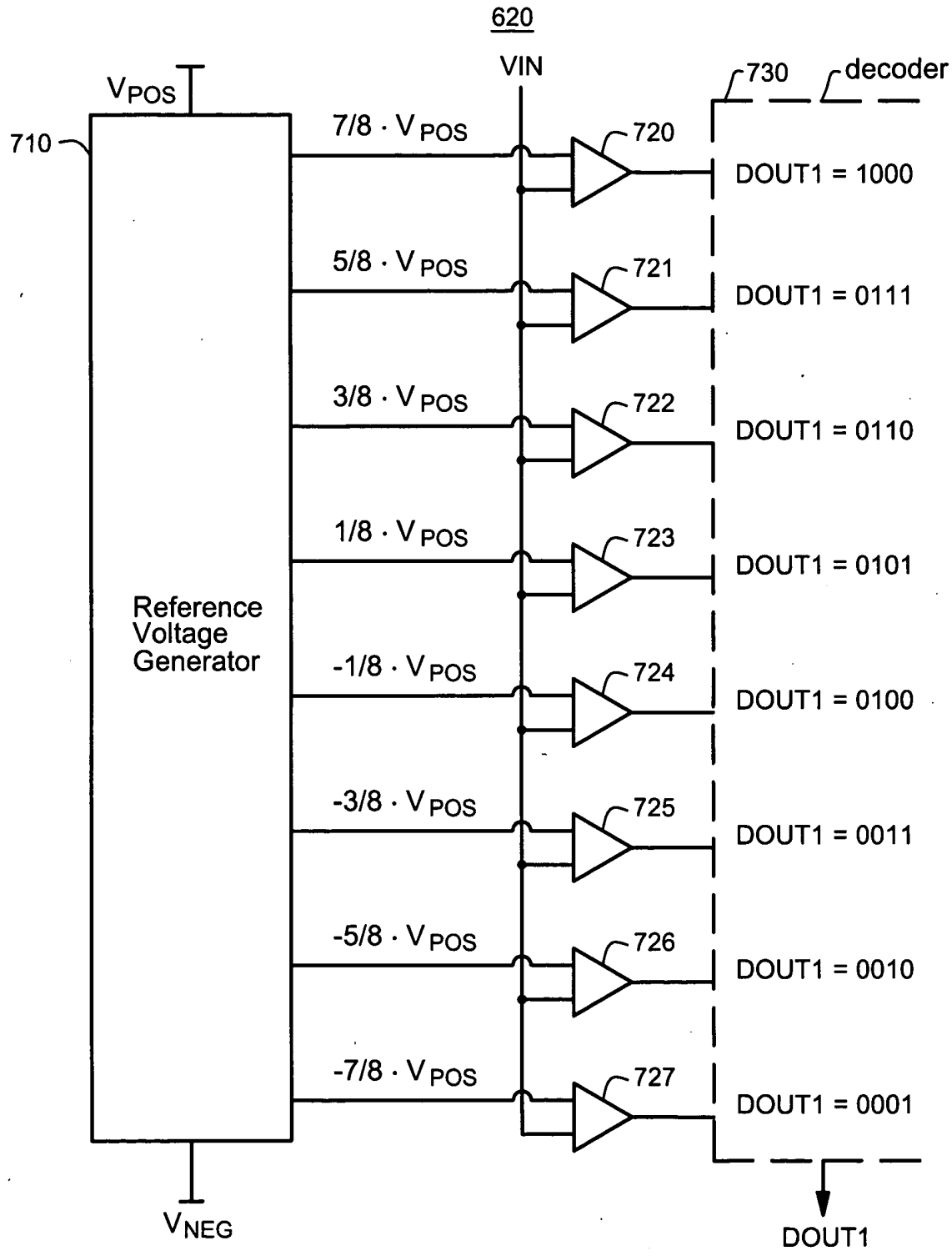

620
VIN
730
decoder
VPOS
710
7/8 · VPOS
720
DOUT1 = 1000
5/8 · VPOS
721
DOUT1 = 0111
3/8 · VPOS
722
DOUT1 = 0110
1/8 · VPOS
723
DOUT1 = 0101
Reference
Voltage
Generator
-1/8 · VPOS
724
DOUT1 = 0100
-3/8 · VPOS
725
DOUT1 = 0011
-5/8 · VPOS
726
DOUT1 = 0010
-7/8 · VPOS
727
DOUT1 = 0001
VNEG
DOUT1

Figure 7

622

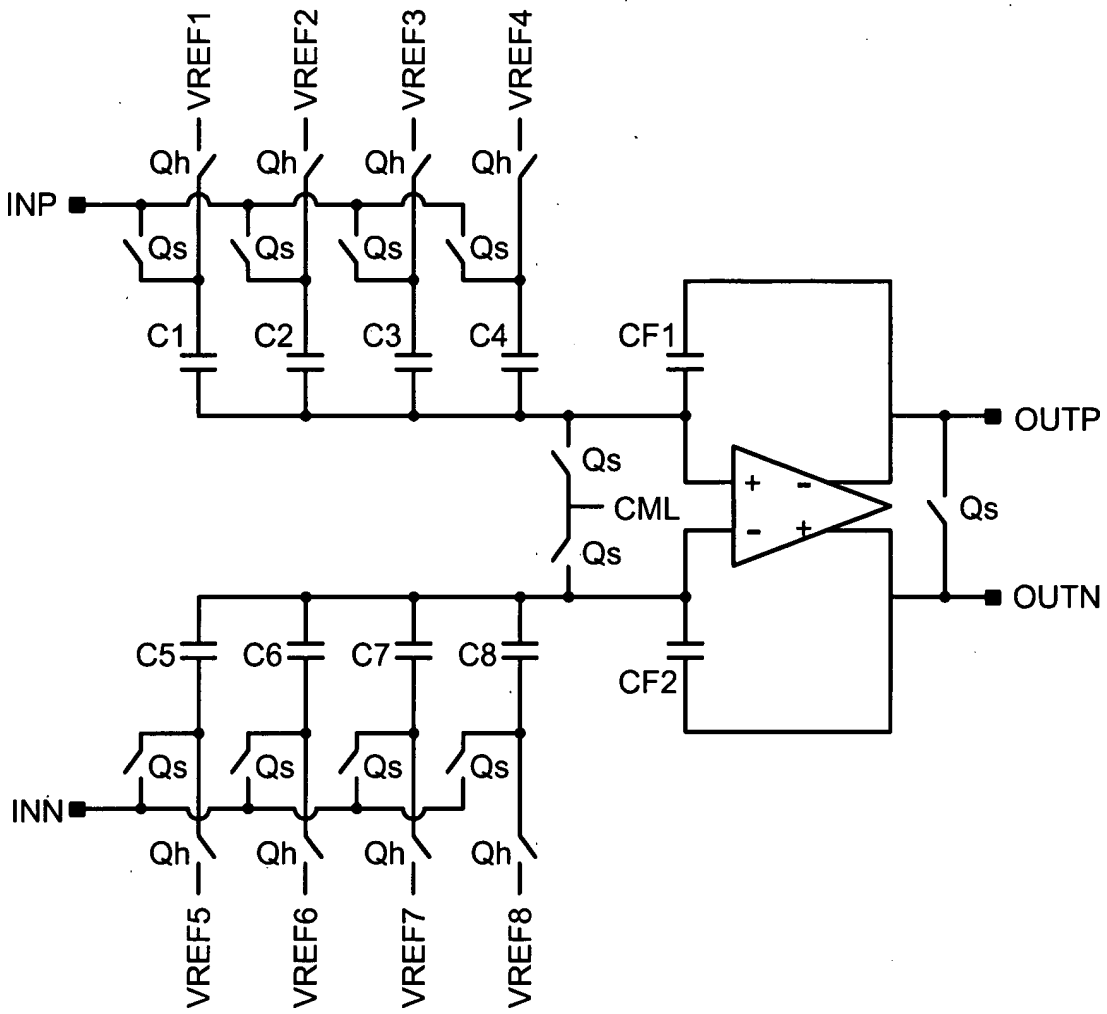


Figure 8A

622

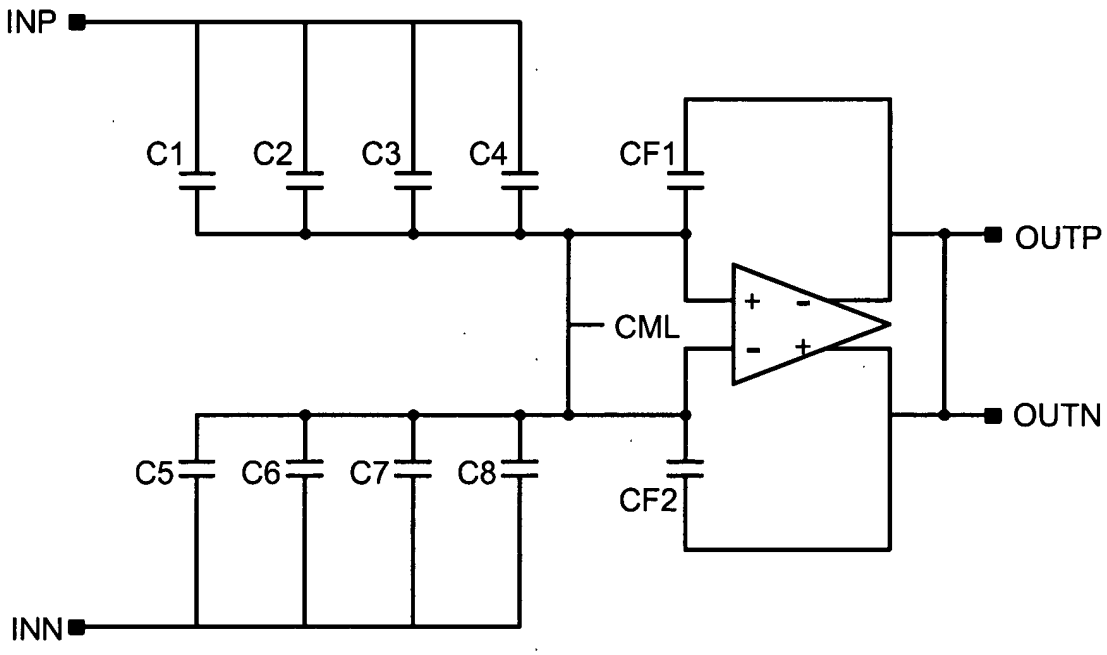


Figure 8B

622

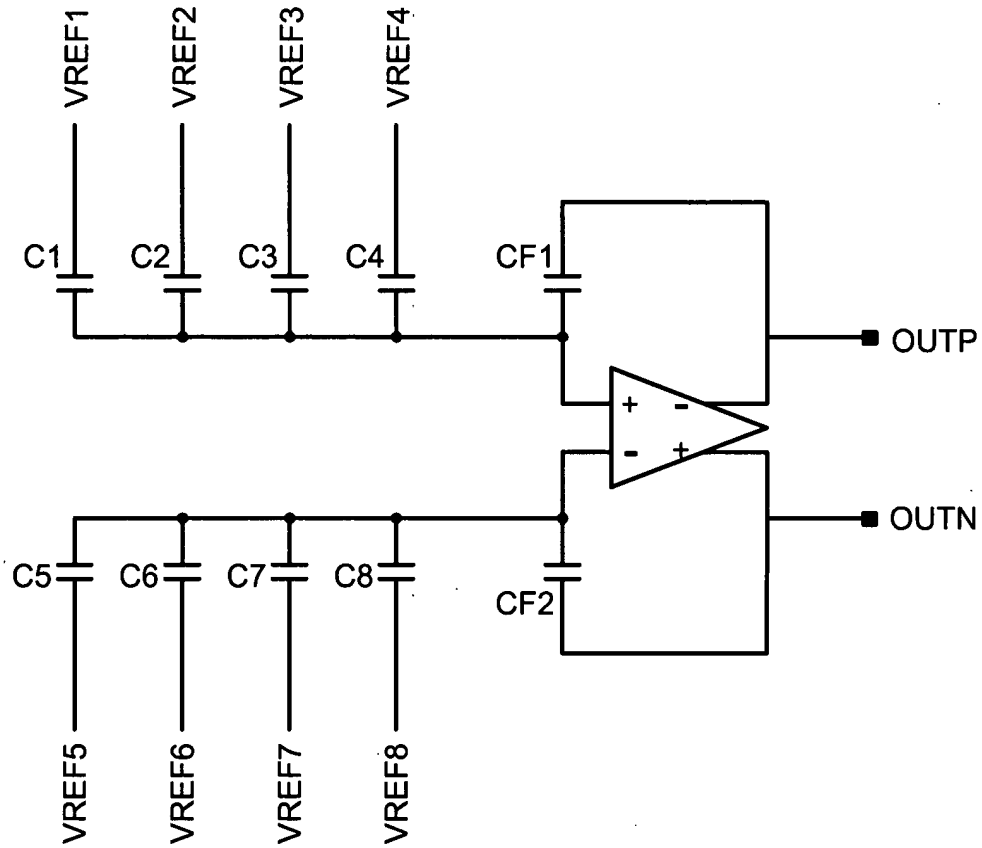


Figure 8C

	VREF1	VREF2	VREF3	VREF4	VREF5	VREF6	VREF7	VREF8	V_{OUT}	DOUT1
7/8 < VIN	0.5	0.5	0.5	0.5	-0.5	-0.5	-0.5	-0.5	$4V_{IN}$- 4	1000
5/8 < VIN < 7/8	0.5	0.5	0.5	0	0	-0.5	-0.5	-0.5	$4V_{IN}$- 3	0111
3/8 < VIN < 5/8	0.5	0.5	0	0	0	0	-0.5	-0.5	$4V_{IN}$- 2	0110
1/8 < VIN < 3/8	0.5	0	0	0	0	0	0	-0.5	$4V_{IN}$- 1	0101
-1/8 < VIN < 1/8	0	0	0	0	0	0	0	0	$4V_{IN}$	0100
-1/8 < VIN < -3/8	-0.5	0	0	0	0	0	0	0.5	$4V_{IN}$+ 1	0011
-3/8 < VIN < -5/8	-0.5	-0.5	0	0	0	0	0.5	0.5	$4V_{IN}$+ 2	0010
-7/8 < VIN < -5/8	-0.5	-0.5	-0.5	0	0	0.5	0.5	0.5	$4V_{IN}$+ 3	0001
VIN < -7/8	-0.5	-0.5	-0.5	-0.5	0.5	0.5	0.5	0.5	$4V_{IN}$+ 4	0000

Figure 9

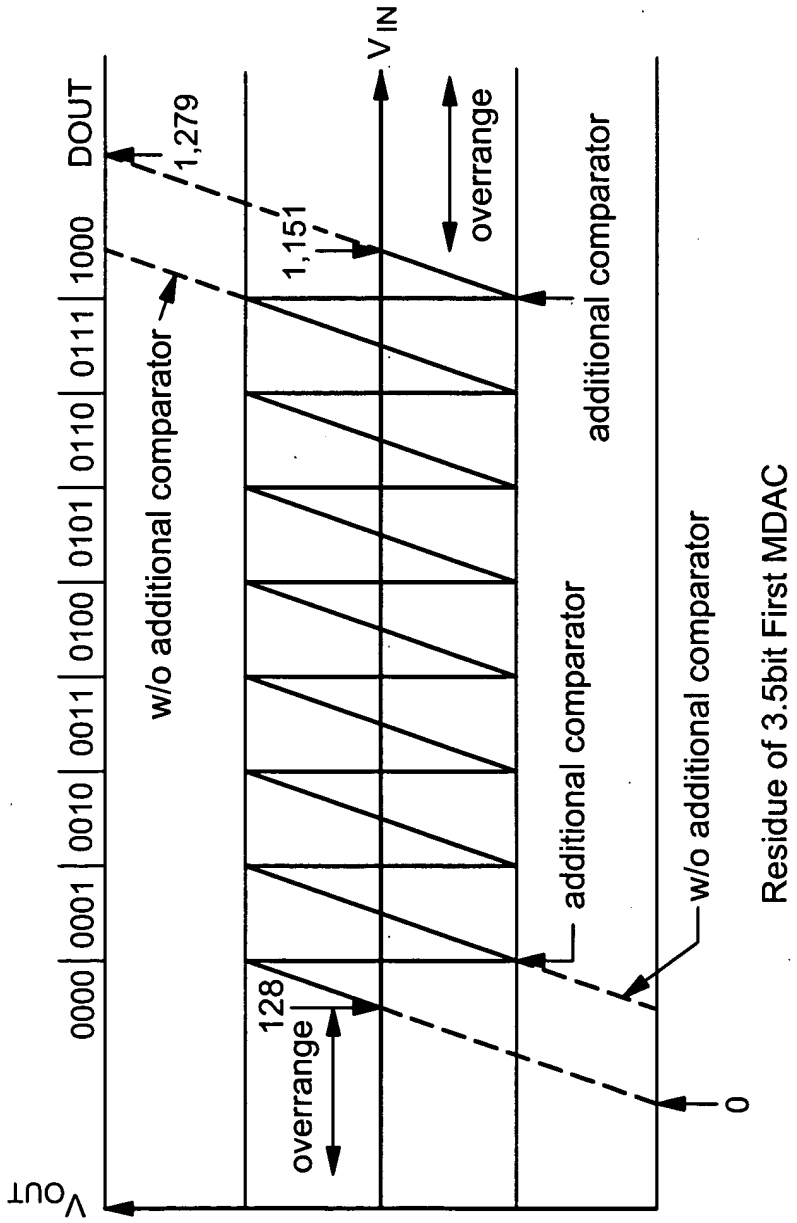

DOUT
0000
0001
0010
0011
0100
0101
0110
0111
1000
1,279
1,151
128
overrange
overrange
w/o additional comparator
additional comparator
additional comparator
w/o additional comparator
Residue of 3.5bit First MDAC
0
V_{IN}
V_{OUT}

Figure 10

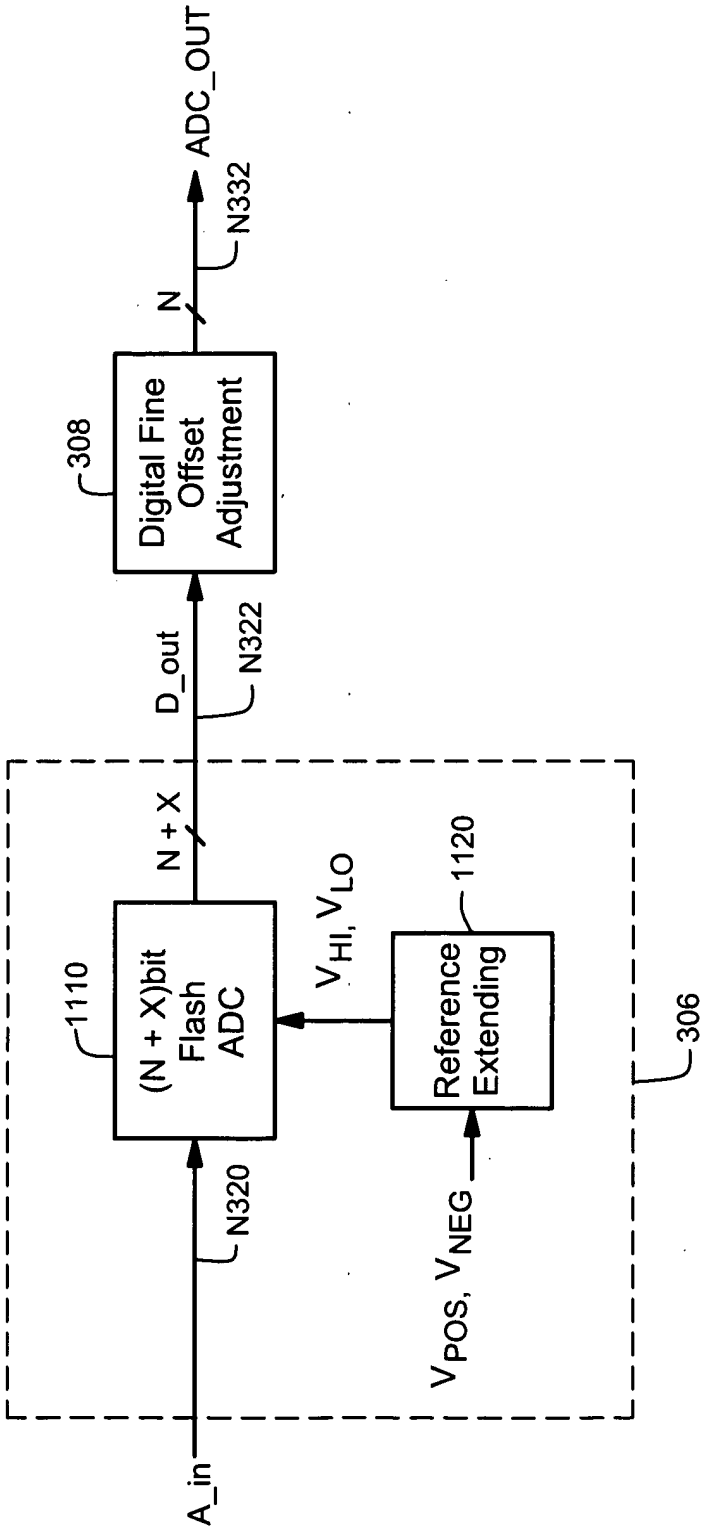

ADC_OUT
N332
N
308
Digital Fine Offset Adjustment
D_out
N322
N + X
1110
(N + X)bit Flash ADC
V_{HI}, V_{LO}
1120
Reference Extending
306
N320
V_{POS}, V_{NEG}
A_in

Figure 11